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21 Symbolic simulation and verification: Enhanced symbolic simulation for efficient verification of embedded array systems

Tao Feng, Li-C. Wang, Kwang-Ting Cheng, Manish Pandey, Magdy S. Abadir

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

Publisher: ACM Press

Full text available: pdf(182.24 KB) Additional Information: full citation, abstract, references, citings

In the past, Symbolic Trajectory Evaluation (STE) was shown to be effective for verifying individual array blocks. However, when applying STE to verify multiple array blocks together as a single system, the run-time OBDD sizes would often blow up. In this paper, we propose using a "dual-rail" symbolic simulation scheme to facilitate the application of STE proof methodology for verifying array systems. The proposed scheme implicitly partitions a given design into control domain and data-path doma ...

22 Have I Really Met Timing? -- Validating PrimeTime Timing Reports with Spice

Tobias Thiel

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 3 DATE '04**

Publisher: IEEE Computer Society

Full text available: pdf(195.50 KB) Additional Information: full citation, abstract, citings, index terms

At sign-off everybody is wondering about how good the accuracy of the static timing analysis timing reports generated with PrimeTime™ really is. Errors can be introduced by STA setup, interconnect modeling, library characterization etc. The claims that path timingcalculated by PrimeTime usually is within a few percent of Spice don't help to ease your uncertainty.When the Signal Integrity features were introduced to PrimeTime there was also a feature added that was hardly announced: PrimeTime can ...

23 A design and validation system for asynchronous circuits

Peter Vanbekbergen, Albert Wang, Kurt Keutzer

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation DAC '95**

Publisher: ACM Press

Full text available: pdf(88.78 KB) Additional Information: full citation, references, citings, index terms

24 Virtual grid symbolic layout

Neil Weste
April 1982 **ACM SIGDA Newsletter**, Volume 12 Issue 2
Publisher: ACM Press
Full text available: pdf(673.63 KB) Additional Information: full citation, abstract, references, index terms

Free form or "stick" type symbolic layout provides a means of simplifying the design of IC subcircuits. To successfully utilize this style of layout, a complete design approach and the necessary tools to support this methodology are required. In particular, one of the requirements of such a design method is the ability to "compact" the loosely specified topology to create a set of valid mask data. This paper presents a new compaction strtegy which uses the concept o ...

25 Self-test methodology for at-speed test of crosstalk in chip interconnects

Xiaoliang Bai, Sujit Dey, Janusz Rajski
June 2000 **Proceedings of the 37th conference on Design automation DAC '00**
Publisher: ACM Press
Full text available: pdf(113.37 KB) Additional Information: full citation, abstract, references, citings, index terms

The effect of crosstalk errors is most significant in high-performance circuits, mandating at-speed testing for crosstalk defects. This paper describes a self-test methodology that we have developed to enable on-chip at-speed testing of crosstalk defects in System-on-Chip interconnects. The self-test methodology is based on the Maximal Aggressor Fault Model [13], that enables testing of the interconnect with a linear number of test patterns. To enable self-testing of the interconnects, we h ...

26 Virtual grid symbolic layout

Neil Weste
June 1981 **Proceedings of the 18th conference on Design automation DAC '81**
Publisher: IEEE Press
Full text available: pdf(708.40 KB) Additional Information: full citation, abstract, references, citings, index terms

Free form or "stick" type symbolic layout provides a means of simplifying the design of IC subcircuits. To successfully utilize this style of layout, a complete design approach and the necessary tools to support this methodology are required. In particular, one of the requirements of such a design method is the ability to "compact" the loosely specified topology to create a set of valid mask data. This paper presents a new compaction strategy which uses the concept o ...

27 Transient fault detection via simultaneous multithreading

Steven K. Reinhardt, Shubhendu S. Mukherjee
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture ISCA '00**, Volume 28 Issue 2
Publisher: ACM Press
Full text available: pdf(151.56 KB) Additional Information: full citation, abstract, references, citings, index terms

Smaller feature sizes, reduced voltage levels, higher transistor counts, and reduced noise margins make future generations of microprocessors increasingly prone to transient hardware faults. Most commercial fault-tolerant computers use fully replicated hardware components to detect microprocessor faults. The components are lockstepped (cycle-by-cycle synchronized) to ensure that, in each cycle, they perform the same operation on the same inputs, producing the same outputs in the abs ...

28 Guidance for the use of the Ada programming language in high integrity systems

B. A. Wichmann
July 1998 **ACM SIGAda Ada Letters**, Volume XVIII Issue 4
Publisher: ACM Press
Full text available: pdf(2.93 MB) Additional Information: full citation, abstract, citings, index terms

This paper is the current result of a study by the ISO HRG Rapporteur group which is being circulated for comment. Many people have contributed to this, but those who have either attended two recent meetings of group or have made substantial e-mail comments are: Praful V Bhansali (Boeing, USA), Alan Burns (University of York, UK), Bernard Carre' (Praxis Critical Systems, UK), Dan Craigen (ORA, Canada), Nick Johnson MoD, UK), Stephen Michell (Canada), Gilles Motet (DGEI/INSA, France), George Roma ...

29 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse
December 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 4
Publisher: ACM Press
Full text available: pdf(5.49 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

30 FPGA circuit design and layout: Design, layout and verification of an FPGA using automated tools

Ian Kuon, Aaron Egier, Jonathan Rose
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays FPGA '05**
Publisher: ACM Press
Full text available: pdf(705.58 KB) Additional Information: full citation, abstract, references, citings, index terms

Creating a new FPGA is a challenging undertaking because of the significant effort that must be spent on circuit design, layout and verification. It currently takes approximately 50 to 200 person years from architecture definition to tape-out for a new FPGA family. Such a lengthy development time is necessary because the process is primarily done manually. Simplifying and shortening the design process would be advantageous since it could reduce the time to market for new FPGAs while also enhanci ...

Keywords: FPGA, PLD, automatic layout, programmable logic

31 Hierarchical circuit extraction with detailed parasitic capacitance

Gary M. Tarolli, William J. Herman
June 1983 **Proceedings of the 20th conference on Design automation DAC '83**
Publisher: IEEE Press
Full text available: pdf(655.70 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a hierarchical MOS layout verification program called IV. IV extracts a circuit netlist from a MOS layout and then compares this netlist to a reference circuit netlist obtained from a schematic. The circuit extraction phase of IV is described in detail. A unique characteristic of the program is the treatment of parasitic capacitance. IV is

currently being used in a production environment to extract circuits in a variety of NMOS and CMOS processes.

32 Evolution of the engineering design system data base

Jere L. Sanborn

January 1982 **Proceedings of the 19th conference on Design automation DAC '82**

Publisher: IEEE Press

Full text available: pdf(409.73 KB) Additional Information: full citation, abstract, references, citings, index terms

The IBM Engineering Design System is a corporate-wide electronic design automation system used for the development of the 3081 and other machines incorporating LSI chips and their carriers. Initially planned in the late 1960s, the system has evolved to respond to a changing set of requirements. This paper describes the evolution of the system data base, as well as the steps taken to ensure the integrity of the data and the correctness of the design.

33 Reunion: Complexity-Effective Multicore Redundancy

Jared C. Smolens, Brian T. Gold, Babak Falsafi, James C. Hoe

December 2006 **Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture MICRO 39**

Publisher: IEEE Computer Society

Full text available: pdf(305.50 KB) Additional Information: full citation, abstract, index terms

To protect processor logic from soft errors, multicore redundant architectures execute two copies of a program on separate cores of a chip multiprocessor (CMP). Maintaining identical instruction streams is challenging because redundant cores operate independently, yet must still receive the same inputs (e.g., load values and shared-memory invalidations). Past proposals strictly replicate load values across two cores, requiring significant changes to the highly-optimized core. We make the key obs ...

34 Virtual grid symbolic layout

N. Weste

June 1988 **Papers on Twenty-five years of electronic design automation 25 years of DAC**

Publisher: ACM Press

Full text available: pdf(872.99 KB) Additional Information: full citation, references, index terms

35 Workstations (panel discussion): a complete solution to the VLSI designer?

Prathima Agrawal, Frederick L. Cohen, Chet Palesko, Hung-Fai Stephen Law, Mark Miller, Mike Price, David W. Smith, Nicholas P. Van Brunt

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation DAC '85**

Publisher: ACM Press

Full text available: pdf(759.20 KB) Additional Information: full citation, abstract, index terms

The dynamics of today's electronics industry introduces enormous pressure on chip designers to come up with chip designs in a very limited time. This is due partly to the short life cycle of application specific products in the marketplace. The availability of powerful graphics processors and microprocessors with processing powers comparable to minicomputers has introduced several stand alone workstations into the design arena. Designer productivity is improved to a great extent by the prov ...

36 Balancing performance and flexibility with hardware support for network architectures

Ilija Hadžić, Jonathan M. Smith

November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4
Publisher: ACM Press
Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

37 ADL: An algorithmic design language for integrated circuit synthesis
W. H. Evans, J. C. Ballegeer, Nguyen H. Duyet
June 1984 **Proceedings of the 21st conference on Design automation DAC '84**
Publisher: IEEE Press
Full text available: pdf(659.93 KB) Additional Information: full citation, abstract, references, citings, index terms

The Algorithmic Design Language (ADL), provides a means to procedurally describe the functional, circuit, schematic and mask aspects of integrated circuits. The constructs of this language have been coded in the C language and are intended for application to IC design. C programs that incorporate ADL routines are executed to build a data base from which CIF files, input files to circuit simulation programs or a textual representation of ADL's own highly structured data base can be generated ...

38 Formal hardware specification languages for protocol compliance verification
Annette Bunker, Ganesh Gopalakrishnan, Sally A. Mckee
January 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 1
Publisher: ACM Press
Full text available: pdf(217.90 KB) Additional Information: full citation, abstract, references, index terms, review

The advent of the system-on-chip and intellectual property hardware design paradigms makes protocol compliance verification increasingly important to the success of a project. One of the central tools in any verification project is the modeling language, and we survey the field of candidate languages for protocol compliance verification, limiting our discussion to languages originally intended for hardware and software design and verification activities. We frame our comparison by first construc ...

Keywords: Esterel, Heterogeneous Hardware Logic, Hierarchical Annotated Action Diagrams, Java, Lava, Live Sequence Charts, Message Sequence Charts, Objective VHDL, OpenVera, Property Specification Language, SpecC, Specification and Description Language, Statecharts, SystemC, SystemVerilog, The Unified Modeling Language, e, hardware monitors, timing diagrams

39 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Publisher: ACM Press
Full text available: pdf(5.28 MB) Additional Information: full citation

40 SubGemini: identifying subcircuits using a fast subgraph isomorphism algorithm

Miles Ohlrich, Carl Ebeling, Eka Ginting, Lisa Sather

July 1993 **Proceedings of the 30th international conference on Design automation DAC '93**

Publisher: ACM Press

Full text available: pdf(822.00 KB) Additional Information: full citation, references, citings, index terms

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